REMARKS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 2-5, 7-10, and 12-21 are pending in this case. Claim 7 is amended herein.

The Examiner did not address claims 19-21 which have not been cancelled or withdrawn. Presumably, claims 19-21 remain allowed.

The Examiner rejected claims 2, 3, 7-9, 13, 15 and 16 under 35 U.S.C. 102(e) as being anticipated by Kim et al. (2003/0058678).

Applicant respectfully submits that claim 2 is unanticipated by Kim as there is no disclosure or suggestion in Kim of a recrystallized polysilicon layer located over a gate electrode layer. Kim teaches an auxiliary polysilicon layer 41. There is no suggestion that polysilicon layer 41 of Kim is "recrystallized" (i.e., deposited as an amorphous layer and recrystallized). Accordingly, Applicant respectfully submits that claim 2 and the claims dependent thereon are unanticipated by Kim.

Applicant respectfully submits that claims 5 and 7 and the claims dependent thereon are similarly unanticipated by Kim.

Applicant respectfully submits that claim 7 if further unanticipated by Kim as there is no disclosure or suggestion of the recrystallized polysilicon layer is located directly on the polysilicon gate layer. Kim teaches a capacitor with underling polysilicon layer 41 formed on a polysilicon plug 25 instead of on the gate 13 as claimed.

Applicant respectfully submits that claim 9 is unanticipated by Kim as there is no disclosure or suggestion in Kim of forming an amorphous silicon layer over a substrate and changing the amorphous silicon layer to a recrystallized polysilicon layer by subjecting the amorphous silicon layer to an annealing process, the annealing process causing the amorphous silicon layer to become the recrystallized polysilicon layer. Kim teaches forming a polysilicon layer 41. This is presumably a polycrystalline silicon layer as is standard in the art. There is no suggestion that the polysilicon layer 41 of Kim is a amorphous silicon layer. Nor is there any teaching of an anneal to change an amorphous silicon layer to a recrystallized polysilicon layer. The only anneal taught near this point in the process in Kim is for creating the silicide. Accordingly, Applicant respectfully submits that claim 9 and the claims dependent thereon are unanticipated by Kim.

The Examiner rejected claim 5 under 35 U.S.C.§ 103(a) as being unpatentable over Kim et al. (2003/0058678) in view of Voutsas et al. (6,642,092).

Applicant respectfully submits that claim 5 is patentable over Kim in view of Voutsas as there is no disclosure or suggestion in the references of a recrystallized polysilicon layer located over a gate electrode layer. Kim teaches an auxiliary polysilicon layer 41. There is no suggestion that polysilicon layer 41 of Kim is "recrystallized" (i.e., deposited as an amorphous layer and recrystallized). Accordingly, Applicant respectfully submits that claim 5 and the claims dependent thereon are patentable over Kim in view of Voutsas.

The Examiner rejected claims 10, 12, 14 and 18 under 35 U.S.C.§ 103(a) as being unpatentable over Kim et al. (2003/0058678) as applied to claims 9 and 13 above, further in view of Voutsas et al. (6,642,092).

Applicant respectfully submits that claims 10, 12, 14, and 18 are patentable over Kim in view of Voutsas for the same reasons discussed above relative to claim 9 from which these claims ultimately depend.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 2-5, 7-10, and 12-21. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

/Jacqueline J Garner/

Jacqueline J. Garner
Reg. No. 36,144

Texas Instruments Incorporated
P. O. Box 655474, M.S. 3999
Dallas, Texas 75265
Phone: (214) 532-9348
Fax: (972) 917-4418